REMARKS

Claims 15-39 are pending. Claims 15-29 have been withdrawn. In the Office Action dated July 13, 2005, Claim 30 was rejected under 35 U.S.C. § 112, first paragraph, Claims 30, 31, 34-29 under 35 U.S.C. § 102, and Claims 30-34 under 35 U.S.C. § 103. Further, the Examiner rejected claim 36-39 under 35 U.S.C. §112, second paragraph.

Applicants have amended claims pursuant to 37 CFR § 1.111. Applicants hereby respectfully request reconsideration of the invention in view of the foregoing amendments and the following remarks.

OBJECTION OF DRAWINGS UNDER 37 CFR §1.83

The Office Action objected to the drawings under 37 CFR §1.83(a) as not showing every feature of the invention specified in the claims. Applicants hereby respectfully traverse this objection.

With reference to Figure 2 of the present invention, channel I/O 210 is illustrated with Bidirectional Data Bus 1 and Bidirectional Data Bus 2. Likewise, channel I/O 212 is also illustrated with Bidirectional Data Bus 1 and Bidirectional Data Bus 2. Since the bidirectional data buses may be used to convey information to and from each of the channel I/Os, Applicants respectfully submit that the first and second data sources are adequately illustrated in the figures.

REJECTION OF CLAIMS UNDER 35 U.S.C. § 112, FIRST PARAGRAPH

The Office Action rejected Claim 30 as failing to comply with the written description requirement. Specifically, the Office Action states that the application does not support claim language reciting "a first channel processor coupled to first and second data sources...a second channel processor coupled to first and second data sources...wherein the first and second channel processor control data from data sources..." Applicants hereby respectfully traverse this rejection.

Applicants respectfully submit the invention discloses a liquid crystal display system that includes a two channel/four display concept having a first channel processor 202, and a second channel processor 204, and four tiles 206-209 (Display 1-4). As illustrated in FIGURE 2 of the present application, the first channel processor 202 is coupled to channel I/O 210, and the second channel processor 204 is coupled to channel I/O 212. Channel I/Os 210 and 212 each use one or more bidirectional data buses to convey information to and from the channel I/Os, and in turn, to and from processor 202 and processor 204, respectively. Thus, Applicants respectfully submit that the first and second data sources are supported by the specification.

Furthermore, Processors 202 and 204, which may include data output and graphical processors, control the display outputs to displays 206-209 (Display 1-4). Therefore, Applicants respectfully submit that the application supports the claims limitations of Claim 30.

The Office Action further rejected Claims 36-39 as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Applicants have amended Claims 36-39, and respectfully submit that the amendments fully address these rejections.

REJECTION OF CLAIMS UNDER 35 U.S.C. § 102

The Examiner rejected Claims 30 and 35-39 as being anticipated by Nishida. In particular, the Examiner asserts that Nishida discloses a channelization system comprising a first channel processor 51-53 coupled to first and second data sources and to *first and second* liquid crystal display units; and a second channel processor 51-53 coupled to the first and second data source and to *third and fourth* liquid crystal display units, wherein the first and second channel process control the data from the data sources displaying data from the same data source to present on the respectfully coupled display.

Applicants respectfully traverse this rejection, and submit that the channel processor 51-53 disclosed in Nishida is not coupled to a plurality of liquid display units. Instead, the channel

processor 51-53 disclosed in Nishida is coupled either to a single display element within a display unit (Figure 3), or in the alternative, coupled to a plurality of pixels that make up one display unit (Figure 9, 19). As a result, Applicants submit that Nishida does not disclose a channel processor that is coupled to a plurality (first and second, or third and fourth) of liquid crystal display units, in contrast to the present invention. Therefore, Applicants submit that Claim 30 is allowable over the cited reference.

Because Claims 35-39 depend from allowable independent Claim 30, they are allowable for the same reason that makes their corresponding independent claim allowable.

REJECTION OF CLAIMS UNDER 35 U.S.C. § 103

The Examiner rejected Claims 30-34 as being unpatentable over Orava et al. (Orava) in view of Seraphim et al. (Seraphim). The Examiner states that Orava teaches or suggests a channelization system comprising a first channel processor coupled to first and second data sources, and a second channel processor coupled to first and second data sources. Applicants respectfully traverse this rejection.

Orava discloses a semiconductor pixel imaging device for use as an image sensor and imaging systems and methods utilizing the pixel semiconductor imaging device. Applicants submit that Orava discloses an image processor, coupled to a single data source (Active-pixel Semiconductor Imaging Device (ASID) 16; FIGURE 1). FIGURES 2-9 and lines 23-46 merely disclose the pixel detectors for detecting radiation energy, and the associated circuits, within the imaging device ASID 16. Thus, Applicants submits that Orava or Seraphim fail to teach or suggest, alone or in combination, connecting each of the image processors to multiple data sources.

Further, the Examiner states that Orava teaches or suggests a channelization system comprising a first channel processor coupled to first and second liquid crystal display units, and a

second channel processor coupled to third and fourth data display units. Applicants also respectfully traverse this rejection.

Orava discloses a semiconductor pixel imaging device for use as an image sensor and imaging systems and methods utilizing the pixel semiconductor imaging device. Applicants submit Orava discloses an image processor connected to a single display 32 (FIGURE 1). Thus, Applicants submit that Orava or Seraphim fail to teach or suggest, alone or in combination, connecting each of the image processors to multiple liquid crystal display units.

Therefore, Applicants submit that Claim 30 is allowable over the cited references. Because Claims 31-34 depend from allowable independent Claim 30, they are allowable for the same reasons for that make their corresponding independent claim allowable.

CONCLUSION

Applicants respectfully submit that all of the claims of the pending application are now in condition for allowance over the cited references. Accordingly, Applicants respectfully request withdrawal of the rejections, allowance, and early passage through issuance. If the Examiner has any questions, the Examiner is invited to contact the Applicants' agent listed below.

Respectfully submitted,

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MAIL CERTIFICATE

I hereby certify that this communication is being deposited with the United States Postal Service via first class mail under 37 C.F.R. § 1.08 on the date indicated below addressed to: MAIL STOP AMENDMENT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

10/7/05
Date of Deposit

Michelle J. Carman